REMARKS

In office action dated 6 November 2002, the Examiner rejects claims 1-9 (all pending claims). In response to the rejections, Applicants amend claims 1,4, and 7. Claims 2-3,5-6, and 8-9 are canceled. Applicants also respectfully traverse the Examiners rejections. Claims 1,4,and 7 remain in the application. In light of the amendments and following argument applicants respectfully request that this Application be allowed.

Applicants have amended claims 1, 4, and 7 to include the substrate upon which the array of cells is disposed, isolation wells that include each byte of memory cells, and well isolation transistors that are connected to each isolation cell. Support for this amendment may be found at page 10, line 16- page 11, line 3 of the specification, no new matter has been entered. This amendment is made to recite the well isolation transistor that is used in the reading, writing and erasing of memory cells to reduce current leakage and turn-on drain. The well isolation transistor is used to adjust the voltage applied to each well during an operation.

The Examiner rejects claim 1 under 35 U.S.C. §102 (b) as being anticipated by U.S. Patent Number 5,949,718 issued to Randolph et al. (Randolph). Claim 1 has been amend to include a substrate, a plurality of isolation wells in the substrate where each isolation well includes a portion of the transistors associated with a byte of data and a well isolation transistor that connects to each of the isolation wells. While Randoph does teach the connections of nonvolatile memory transistors in the manner described, Randolph does not teach providing isolation wells or isolation well transistors for adjusting a voltage applied to the isolation wells. However, as stated above the use of isolation wells and adjusting voltage applied to the isolation wells

help reduce leakage and turn-on drain. Thus, amended claim 1 is not anticipated by Randolph and the rejection of claim 1 must be removed.

Claims 2 and 3 are rejected as being unpatentable under 35 U.S.C. §103(a) as being unpatentable over Randolph in view of U.S. Patent Number 6,243,298 issued to Lee et al. (Lee). Since claim 1 has been amended to include features of claims 2 and 3, this rejection is addressed. As stated above, Randolph does teach the isolation wells and isolation transistors of recited in amended claim 1.

Lee also does not teach the isolation wells and well isolation transistors recited in amended claim 1. Specifically, Lee does not teach isolation well including the cells of a byte of data. Instead, Lee is silent as to how the isolation wells are disposed. Thus, Lee does not teach the recitation of isolation wells in claim 1. Thus, the combination of Randoph and Lee do not teach amended claim 1.

Claims 4 and 7 merely recite other types of memory and have been amended similar to claim1. Thus, claims 4 and 7 are allowable for at least the same reasons as amended claim 1. Thus, the rejections of amended claims 4 and 7 should be removed.

If the examiner has any questions regarding this response or the application in general, the Examiner may telephone the undersigned at 775-586-9500.

Respectfully submitted,
Sierra Patent Group, Ltd.

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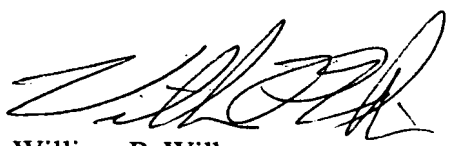

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Marked up Version of the Amendments

1. (Amended) An array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns comprising:

a substrate upon which said array is deposited;

a [wordline] plurality of wordlines wherein each of said plurality of wordlines is associated with [each row] a one of said plurality of rows in [of] the array;

a [bitline] plurality of bitlines wherein each of said plurality of bitlines is associated with [each column of] one of said plurality of columns in the array;

a plurality of nonvolatile memory transistors, each of said nonvolatile memory transistors associated with [one row and one column] a one of said plurality of rows and a one of said plurality of columns in the array, each [nonvolatile memory transistor] one of said plurality of nonvolatile memory transitors having a source, a drain, a floating gate and a control gate, the control gate of each one of said plurality of nonvolatile memory [transistor] transistors coupled to the one of said plurality of wordlines [with which its row is associated] of said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistor, the drain of each one of said plurality of nonvolatile memory [transistor] transistors coupled to the one of said plurality of bitlines [with which its column is associated;] of said one of said plurality of columns associated with said one of said plurality of nonvolatile memory transistors, the source of each one of said plurality of nonvolatile memory [transistor in a row of the array coupled together] being couple to the source of each of said other ones of said plurality of nonvolatile memory

transistors in said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistors; [and]

a plurality of source [transistor associated with each row of the array] transistors wherein each one of said plurality of [said] source [transistor] transistors has [having] a gate coupled to [the one of said] a one of said plurality of wordlines [with which its row is associated], a source coupled to a source potential line, and a drain coupled to the sources of each of said plurality of nonvolatile memory [transistor with which its row is;] transistors associated with said one of said plurality of rows associated with said wordline coupled to said source of said one of said plurality of source transistors;

a plurality of isolation well in said substrate wherein a portion of said plurality of nonvolatile memory transistors associated with a byte of data are disposed in each of said plurality of isolation wells; and

a plurality of well selection transistors wherein each one of said plurality of well selection transistors is connected to a one of said plurality of isolation wells.

4. (Amended) An array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns comprising:

a substrate upon which said array is deposited;

a [wordline] plurality of wordlines wherein each of said plurality of wordlines is associated with [each row] a one of said plurality of rows in [of] the array;

a [bitline] plurality of bitlines wherein each of said plurality of bitlines is associated with [each column of] one of said plurality of columns in the array;

a plurality of nonvolatile memory transistors, each of said nonvolatile memory transistors associated with [one row and one column] a one of said plurality of rows and a one of said plurality of columns in the array, each [nonvolatile memory transistor] one of said plurality of nonvolatile memory transistors having a source, a drain, a floating gate and a control gate, the control gate of each one of said plurality of nonvolatile memory [transistor] transistors coupled to the one of said plurality of wordlines [with which its row is associated] of said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistor, the drain of each one of said plurality of nonvolatile memory [transistor] transistors coupled to the one of said plurality of bitlines [with which its column is associated;] of said one of said plurality of columns associated with said one of said plurality of nonvolatile memory transistors, the source of each one of said plurality of nonvolatile memory [transistor in a row of the array coupled together] being couple to the source of each of said other ones of said plurality of nonvolatile memory transistors in said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistors; [and]

a plurality of source [transistor associated with each row of the array] transistors wherein each one of said plurality of [said] source [transistor] transistors has [having] a gate coupled to [the one of said] a one of said plurality of wordlines [with which its row is associated], a source coupled to a source potential line, and a drain coupled to the sources of each of said plurality of nonvolatile memory [transistor with which its row is;] transistors associated with said one of said plurality of rows associated with said wordline coupled to said source of said one of said plurality of source transistors;

a plurality of isolation wells in said substrate wherein a portion of said plurality of nonvolatile memory transistors associated with a byte of data are disposed in each of said plurality of isolation wells; and

a plurality of well selection transistors wherein each one of said plurality of well selection transistors is connected to a one of said plurality of isolation wells.

7. (Amended) An array of one-time programmable nonvolatile memory cells arranged in a plurality of rows and a plurality of columns comprising:

a substrate upon which said array is deposited;

a [wordline] plurality of wordlines wherein each of said plurality of wordlines is associated with [each row] a one of said plurality of rows in [of] the array;

a [bitline] plurality of bitlines wherein each of said plurality of bitlines is associated with [each column of] one of said plurality of columns in the array;

a plurality of nonvolatile memory transistors, each of said nonvolatile memory transistors associated with [one row and one column] a one of said plurality of rows and a one of said plurality of columns in the array, each [nonvolatile memory transistor] one of said plurality of nonvolatile memory transitors having a source, a drain, a floating gate and a control gate, the control gate of each one of said plurality of nonvolatile memory [transistor] transistors coupled to the one of said plurality of wordlines [with which its row is associated] of said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistor, the drain of each one of said plurality of nonvolatile memory [transistor] transistors coupled to the one of said plurality of bitlines [with which its column is associated;]

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of said one of said plurality of columns associated with said one of said plurality of nonvolatile memory transistors, the source of each one of said plurality of nonvolatile memory [transistor in a row of the array coupled together] being couple to the source of each of said other ones of said plurality of nonvolatile memory transistors in said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistors; [and]

a plurality of source [transistor associated with each row of the array] transistors wherein each one of said plurality of [said] source [transistor] transistors has [having] a gate coupled to [the one of said] a one of said plurality of wordlines [with which its row is associated], a source coupled to a source potential line, and a drain coupled to the sources of each of said plurality of nonvolatile memory [transistor with which its row is;] transistors associated with said one of said plurality of rows associated with said wordline coupled to said source of said one of said plurality of source transistors;

a plurality of isolation well in said substrate wherein a portion of said plurality of nonvolatile memory transistors associated with a byte of data are disposed in each of said plurality of isolation wells; and

a plurality of well selection transistors wherein each one of said plurality of well selection transistors is connected to a one of said plurality of isolation wells.